AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (previously presented) An apparatus comprising:

a first scoreboard operating as an issue scoreboard to scoreboard instructions for issue;

a second scoreboard operating as a replay scoreboard to scoreboard instructions which have passed a replay stage in a pipeline; and

a control circuit coupled to the first scoreboard and the second scoreboard, wherein the control circuit is configured to update the first scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into the pipeline, and wherein the control circuit is configured to update the second scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing the replay stage of the pipeline, wherein the control circuit, in response to a replay of a second instruction by checking operands of the second instruction against the second scoreboard, is configured to copy contents of the second scoreboard to the first scoreboard.

2. (previously presented) The apparatus as recited in claim 1 further comprising a third scoreboard coupled to the control circuit and operating as a graduation scoreboard to scoreboard instructions which have passed a graduation stage of the pipeline, wherein the control circuit is configured to update the third scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing the graduation stage of the pipeline, wherein the control circuit, in response to an exception for a third instruction, is configured to copy contents of the third scoreboard to the first and second scoreboards.

3. (previously presented) The apparatus as recited in claim 2 wherein the control circuit is configured to copy the contents of the third scoreboard to the second scoreboard and to subsequently copy contents of the second scoreboard to the first scoreboard.

4. (previously presented) The apparatus as recited in claim 2 wherein a redirect due to a mispredicted branch instruction is detected at the replay stage, and wherein the control circuit, in response to the redirect, is configured to copy the contents of the second scoreboard to the first scoreboard.

5. (canceled)

6. (previously presented) The apparatus as recited in claim 1 wherein the first scoreboard and the second scoreboard track pending writes to integer registers.

7. (previously presented) The apparatus as recited in claim 6 wherein the control circuit is configured to selectively inhibit issuance of a third instruction dependent on which of a plurality of pipelines to which the third instruction is to be issued if the first scoreboard indicates a write pending to one of the operands of the third instruction.

8. (previously presented) The apparatus as recited in claim 7 wherein, if the third instruction is to be issued to a load/store pipeline of the plurality of pipelines, the control circuit is configured to inhibit issuance of the third instruction if the first scoreboard indicates a write pending to one of the operands of the third instruction.

9. (previously presented) The apparatus as recited in claim 8 wherein, if the third instruction is to be issued to an integer pipeline of the plurality of pipelines, the control circuit is configured to allow issuance of the third instruction even if the first scoreboard indicates a write pending to one of the operands of the third instruction.

10. (previously presented) The apparatus as recited in claim 9 wherein the integer pipeline includes a register read stage which is delayed to align the register read stage with a data forwarding stage of the load/store pipeline.

11. (previously presented) The apparatus as recited in claim 6 wherein the first instruction is a load instruction, and wherein the load instruction passes the replay stage if the load instruction misses in a data cache.

12. (previously presented) The apparatus as recited in claim 1 wherein the control circuit is configured to update the first scoreboard and the second scoreboard to indicate that the write is not pending to the first destination register at a first predetermined clock cycle prior to the first instruction writing the first destination register.

13. (previously presented) The apparatus as recited in claim 12 further comprising a third scoreboard, wherein the control circuit is configured to update the third scoreboard to indicate that the write is pending to the first destination register in response to issuing the first instruction, and wherein the control circuit is configured to update the third scoreboard to indicate that the write to the first destination register is not pending at a second predetermined clock cycle prior to the first instruction writing the first destination register.

14. (previously presented) The apparatus as recited in claim 13 wherein the second predetermined clock cycle is prior to the first predetermined clock cycle.

15. (previously presented) The apparatus as recited in claim 14 wherein the first scoreboard and the second scoreboard track pending writes to floating point registers, and wherein the control circuit is configured to determine whether or not a floating point multiply-add instruction is issuable by checking the multiplicand operands against the first scoreboard and the add operand against the third scoreboard.

16. (previously presented) The apparatus as recited in claim 14 wherein the control circuit is configured to check for a read after write dependency for an instruction to be issued using the first scoreboard and to check for a write after write dependency using the third scoreboard.

17. (previously presented) The apparatus as recited in claim 13 further comprising a fourth scoreboard, wherein the control circuit is configured to update the fourth scoreboard to indicate the write to the first destination register is pending responsive to the first instruction passing the replay stage, and wherein the control circuit is configured to update the fourth scoreboard to indicate that the write to the first destination register is not pending at the second predetermined clock cycle, and wherein the control circuit is configured to copy contents of the fourth scoreboard to the third scoreboard responsive to the replay of the second instruction.

18. (previously presented) A method comprising:

updating a first scoreboard operating as an issue scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into a pipeline;

updating a second scoreboard operating as a replay scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a replay stage of the pipeline, wherein replay is signaled at the replay stage; and

detecting a replay of a second instructions by checking operands of the second instruction against the second scoreboard and in response to the replay of the second instruction, copying a contents of the second scoreboard to the first scoreboard.

19. (previously presented) The method as recited in claim 18 further comprising:

updating a third scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a graduation stage of the pipeline where instructions graduate; and

copying a contents of the third scoreboard to the second scoreboard and to the first scoreboard in response to an exception for a third instruction.

20. (previously presented) The method as recited in claim 19 wherein the copying the contents of the third scoreboard comprises:

copying the contents of the third scoreboard to the second scoreboard; and

copying subsequently contents of the second scoreboard to the first scoreboard.

21. (previously presented) The method as recited in claim 18 further comprising:

detecting a redirect due to a mispredicted branch instruction at the replay stage; and

copying the contents of the second scoreboard to the first scoreboard in response to the redirect.

22. (canceled)

23. (previously presented) The method as recited in claim 18 wherein the first scoreboard and the second scoreboard track pending writes to integer registers.

24. (previously presented) The method as recited in claim 23 further comprising inhibiting selectively issuance of a third instruction dependent on which of a plurality of pipelines to which the third instruction is to be issued if the first scoreboard indicates a write pending to one of the operands of the third instruction.

25. (previously presented) The method as recited in claim 24 wherein the inhibiting selectively comprises:

if the third instruction is to be issued to a load/store pipeline of the plurality of pipelines, inhibiting issuance of the third instruction if the first scoreboard indicates a write pending to one of the operands of the third instruction; and

if the third instruction is to be issued to an integer pipeline of the plurality of pipelines, allowing issuance of the third instruction even if the first scoreboard indicates a write pending to one of the operands of the third instruction.

26. (previously presented) The method as recited in claim 23 wherein the first instruction is a load instruction, and wherein the load instruction passes the replay stage if the load instruction misses in a data cache.

27. (previously presented) The method as recited in claim 18 further comprising updating the first scoreboard and the second scoreboard to indicate that the write is not pending to the first destination register at a first predetermined clock cycle prior to the first instruction writing the first destination register.

28. (previously presented) The method as recited in claim 27 further comprising:

updating a third scoreboard to indicate that the write is pending to the first destination register in response to issuing the first instruction; and

updating the third scoreboard to indicate that the write to the first destination register is not pending at a second predetermined clock cycle prior to the first instruction writing the first destination register.

29. (previously presented) The method as recited in claim 28 wherein the second predetermined clock cycle is prior to the first predetermined clock cycle.

30. (previously presented) The method as recited in claim 29 wherein the first scoreboard and the second scoreboard track pending writes to floating point registers, the method further comprising determining whether or not a floating point multiply-add instruction is issuable by checking the multiplicand operands against the first scoreboard and the add operand against the third scoreboard.

31. (previously presented) The method as recited in claim 29 further comprising:

checking for a read after write dependency for an instruction to be issued using the first scoreboard; and

checking for a write after write dependency using the third scoreboard.

32. (previously presented) The method as recited in claim 28 further comprising:

updating a fourth scoreboard to indicate the write to the first destination register is pending responsive to the first instruction passing the replay stage;

updating the fourth scoreboard to indicate that the write to the first destination register is not pending at the second predetermined clock cycle; and

copying a contents of the fourth scoreboard to the third scoreboard responsive to the replay of the second instruction.

33. (currently amended) A storage media comprising one or more data structures to manufacture a processor:

a first scoreboard operating as an issue ~~scoreborad~~ scoreboard to scoreboard instructions for issue;

a second scoreboard operating as a replay ~~scoreborad~~ scoreboard to scoreboard instructions which have passed a replay stage in a pipeline; and

a control circuit coupled to the first scoreboard and the second scoreboard, wherein the control circuit is configured to update the first scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into the pipeline, and wherein the control circuit is configured to update the second scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing the replay stage of the pipeline, wherein the control circuit, in response to a replay of a second instruction by checking operands of the second instruction against the second scoreboard, is configured to copy contents of the second scoreboard to the first scoreboard.

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Respectfully submitted,

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Date: 1-28-2005

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